04-06-05

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Attorney Docket No. 64,610-043A (YO998-503)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kenneth P. Rodbell
Serial No.: 10/ 055,134
Filed: Jan. 22, 2002
For: Method for Plating Copper conductors and Devices Formed

Group Art Unit: 1753
Examiner: Phasge, Arun S.

Commissioner for Patents
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Feb. 4, 2005.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$250.00
X	other than a small entity	$500.00

Appeal Brief fee due: $ 500.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service
with sufficient postage as Express Mail
Label No. EV 492 466 619 US
in an envelope addressed to Commissioner
for Patents, Alexandria, VA 22313-1450

Kathy Dixon

Dated: April 4, 2005

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of □1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) □ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
□	one month	$ 120.00	$ 60.00
□	two months	$ 450.00	$225.00
□	three months	$ 1,020.00	$510.00
□	four months	$ 1,590.00	$795.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

□ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) □ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 500.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 500.00

6. FEE PAYMENT

___ Attached is a Credit Card Payment Form for the sum of $ 0.00
X Charge Deposit Account No. 50-0510 the sum of $ 500.00
A duplicate copy of this transmittal is attached.

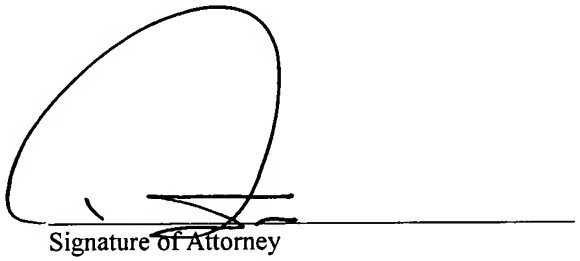
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

_X_ If any additional extension and/or fee is required, this is a request therefor to charge Deposit Account No. 50-0510

And/Or

_X_ If any additional fee for claims is required, please charge Deposit Account No. 50-0510



Signature of Attorney

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re: Application of:

Kenneth P. Rodbell — Group Art Unit: 1753

Serial No: 10/ 055,134 — Examiner: Phasge, Arun S.

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Attorney Docket No.: 64,610-043A (YO998-503)

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 492 466 619 US
Date of Deposit April 4, 2005

I hereby certify that this paper in triplicate is being deposited with the United States Postal Service "Express Mail Post Office To Addressee" service under 37 CFR § 1.10 on the date indicated above and is addressed to: Mail Stop: Appeal-Patent, Commissioner for Patents, Alexandria, VA 22313-1450.

Kathy Dixon

APPEAL BRIEF

Mail Stop: Appeal-Patents
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Appellants appeal in the captioned application from the Examiner's final rejection, dated Nov. 4, 2004 of claims 28-30 under 35 USC §103(a) as being unpatentable over Uzoh et al 6,465,376 and Chidambarrao et al 6,417,572.

It is urged that the rejection be reversed and that all the claims be allowed.

(I) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee of International Business Machines Corporation.

(ii) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellants, the Appellants' legal representative, or the assignee.

(iii) STATUS OF CLAIMS

Claims 28-30 are pending in the application.

Claims 28-30 stand rejected. Claims 28-30 are now on appeal. No claims stand allowed.

(iv) STATUS OF AMENDMENTS

A Request For Reconsideration was filed on Feb. 4, 2005, which contains claim amendments to claim 29.

An Advisory Action was mailed by the Examiner on March 2, 2005 maintaining rejection of all claims.

A Notice of Appeal was filed on Feb. 4, 2005.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a method for plating copper conductors on an electronic substrate in a plating bath kept at a temperature below 18°C with a low dopant concentration resulting in improved resistance transient in plated copper films and devices made by such method.

(Specification, page 1, lines 4-7)

In a preferred embodiment, a method for plating copper conductors on an electronic substrate can be carried out by the operating steps of first providing an electroplating copper bath filled with an electroplating solution, maintaining the electroplating solution at a temperature between about 0°C and about 18°C, and then electroplating a copper layer on the electronic substrate immersed in the electroplating solution.

(Specification, page 5, lines 9-13)

The present invention is further directed to a semiconductor structure of a damascene or dual-damascene interconnect formed by a trench-filling process of electroplated Cu having an as-deposited grain size of not less than .05 μm and a decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C.

(Specification, page 8, lines 1-4)

In the semiconductor structure of a damascene or dual-damascene interconnect, the as-deposited grain size of the electroplated Cu is between about .05 μm and about .15 μm. The grain size of the electroplated Cu after the time period of not more than 30 hours at about 21°C is between about 1.5 μm and about 2 μm.

(Specification, page 8, lines 5-8)

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 28-30 are rejected under 35 USC §103(a) as being unpatentable over Uzoh et al '376 and Chidambarrao et al '572.

(vii) ARGUMENT

CLAIMS 28-30

Claim 28 (specification, page 8, lines 1-4), claim 29 (specification, page 8, lines 5-6) and claim 30 (specification, page 8, lines 6-8) are rejected under 35 USC §103(a) as being unpatentable over Uzoh et al '376 in view of Chidambarrao et al '572. It is contended that Uzoh discloses the claimed damascene interconnect formed by a trench-filling process of electroplating copper including the range of copper grain size as claimed. It is further contended that while Uzoh does not teach a decrease in electrical resistance, such is taught by Chidambarrao in disclosing a relationship between the electrical resistance and the grain size as it relates to the voids in the interconnect.

The rejection of claims 28-30 under 35 USC §103(a) based on Uzoh et al and Chidambarrao et al is improper and must be reversed.

Uzoh et al discloses a method and structure for improving electromigration of chip interconnects wherein a microstructure including a conductive layer of aluminum, copper or alloys thereof on a substrate wherein the layer including metal grains at least about 0.1 microns and barrier material. (See Abstract)

> At col. 4, lines 4-11, Uzoh et al further states:
> "Large grains are always preferably to small grains, as grain boundaries present a fast-diffusion path for electromigration or stress migration (both are interconnect wear out mechanisms). Therefore larger grained damascene interconnects have higher reliability when all other factors are equal. **A typical average aluminum grain size (for fill in submicron trenches) is on order of 0.5 micron, in a lognormal distribution.**"

The present invention, on the other hand, recites a semiconductor structure having interconnects formed of copper with grain size **not less than 0.5 μm** and **a decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C**, as clearly recited in independent claim 28. Contrary to the teaching of Uzoh et al that the average grain size is 0.5 micron, the present invention teaches and claims a grain size of not less than 0.5 micron. Furthermore, no where in Uzoh is taught the unexpected result only discovered by the present invention of having a decrease in electrical resistance of at least 15%.

Chidambarrao et al discloses a process for producing metal interconnections and product in which a process for producing a multi-level semiconductor device that has metal interconnections with insulating passivation layers is disclosed. At col. 4, lines 8-33, Chidambarrao et al states:

> "Methods of reducing the effect of void formation on the electrical resistance of interconnect conductors in multi-level metallization structures having provided by incorporating multiple continuous redundant conductive layers ... Typically, the grain size of the redundant underlayer or overlayer of a multi-layer conductor is much less than the width of the conducting interconnect..."

The Appellants respectfully submit while Chidambarrao et al discussed the general principal of reducing the effect of void formation on the electrical resistance of interconnect conductors, Chidambarrao et al does not specifically teach, as now recited in independent claim 18:

> "interconnect formed by a trench-filling process of electroplated Cu having an as-deposited **grain size of not less than 0.5 μm** and a **decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C.**"

The Appellants respectfully submit that, contrary to the Examiner's contention that Chidambarrao et al shows the relationship between the electrical resistance and the grain size, such relationship is not shown by Chidambarrao and is only shown by the present invention as recited in independent claim 28.

In the Response to Arguments Section of the 11/04/2004 Office Action, the Examiner further argued that "the reference while teaching the average grain size of 0.5 microns further teaches as recited in the remarks, that 'large grains are always preferable to small grains'. Thus one having

ordinary skill in the art would have been motivated to maintain the grain size at 0.5 micron or larger".

The Appellants respectfully submit that such reasoning does not support a §103(a) obviousness rejection since Uzoh teaches that **the average grain size of 0.5 microns, and Uzoh does not teach the minimum grain size of 0.5 microns**, which is only taught by the present invention. When the average grain size is 0.5 microns, then the minimum grain size must be smaller than 0.5 microns taught by Uzoh. The Appellants therefore respectfully submit that it is only the present invention that teaches a minimum grain size must be 0.5 microns, and that, any grain size at less than 0.5 microns would not work. The Appellants therefore respectfully submit that the minimum grain size of 0.5 microns is clearly not taught by Uzoh.

The Examiner further argued that "the Chidambarrao patent teaches that by selection of grain size and reducing void formation, electrical resistance may be controlled (see col. 4, lines 8-33)." The Appellants respectfully submit that such teaching does not even come close to the present invention's teaching of "a decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C." In other words, the present invention clearly defined limitation can not be inferred from the vague and indefinite statement of Chidambarrao.

The rejection of claims 28-30 under 35 USC §103(a) based on Uzoh et al and Chidambarrao et al is improper and must be reversed.

CLOSING

In summary, the Appellants have shown that their claimed invention is fully supported by a body of evidence of non-obviousness. It is respectfully submitted that such evidence of non-obviousness overcomes any showing of obviousness presented by the Examiner. The Appellants therefore respectfully submit that the final rejection of their claims 28-30 is improper under 35 USC §103.

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

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(viii) **CLAIMS APPENDIX**

1. - 27. (Cancelled)

28. (Original) A semiconductor structure of a damascene or dual damascene interconnect formed by a trench-filling process of electroplated Cu having an as-deposited grain size of not less than 0.5 μm and a decrease in electrical resistance of at least 15% after a time period of not more than 30 hours at about 21°C.

29. (Previously Presented) A semiconductor structure of a damascene or dual damascene interconnect according to claim 28, wherein said as-deposited grain size of electroplated Cu is between about 0.5 μm and about 1.5 μm.

30. (Original) A semiconductor structure of a damascene or dual damascene interconnect according to claim 28, wherein said grain size of said electroplated Cu after said time period of not more than 30 hours at about 21°C is between about 1.5 μm and about 2 μm.

(ix) EVIDENCE APPENDIX

None

(x) RELATED PROCEEDINGS APPENDIX

None